A2

[0040] Exemplary voltages for the programming, erase and reading operations of the memory are described in the aforementioned U.S. patent no. 6,355,524.

IN THE CLAIMS

A3

1. (Amended) A method for forming cobalt silicide on a body which has a surface that comprises silicon, the method comprising:

forming a cobalt layer on said surface;

forming a titanium layer over the cobalt layer by ionized physical vapor deposition while the body is attached to a support biased with an AC power of 0 W;

reacting the cobalt with the silicon to form cobalt silicide; and

removing the titanium layer, and if any cobalt has not reacted with the silicon then removing the unreacted cobalt.

Please cancel Claim 2.

A4

3. (Amended) The method of Claim 1 wherein during the titanium layer deposition the distance between a titanium target and the body is at least 140 mm.

4. (Unchanged) The method of Claim 1 wherein the titanium layer is at most 7.5 nm thick.

A5

5. (Amended) The method of Claim 1 wherein said silicon surface is located at a bottom of an opening having an aspect ratio of at least 2.5.

6. (Amended) The method of Claim 5 wherein at least part of a sidewall surface of the opening is made of a dielectric.

Please add the following claim:

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A6

7. (New) The method of Claim 1 wherein the titanium layer is deposited on the cobalt layer to be in contact with the cobalt layer.

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